- Wide Input Voltage Range: 2.7V-14.0V
- Wide Output Voltage Range: 4.5V-14.6V
- Fully Integrated High-side/Low-side Power MOSFETs：13m /11m
- Up to 12A Switch Current and Programmable Peak Current Limit
- Typical Shut-down Current: 1uA
- Programmable Switching Frequency: 200kHz-2.2MHz
- Output Overvoltage Protection at 15.4V
- Feedback Overvoltage Protection at 110% of Reference Voltage
- Selectable PFM or Forced PWM Mode
- Programmable Soft Start
- Thermal Shutdown Protection: 150°C
- Available in DFN-20 3.5mmx4.5mm Package

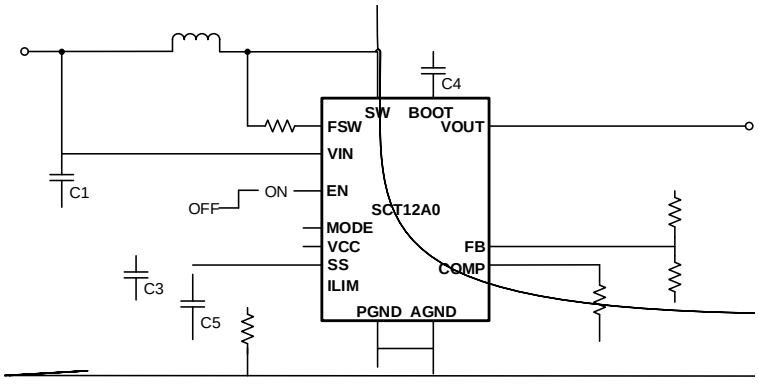
- Bluetooth Audio
- Power Banks
- POS System
- E-Cigarette
- USB Power Delivery

The SCT12A0 is a high efficiency synchronous boost converter with fully integrated a 13 high-side MOSFET and an low-side MOSFET, supporting 2.7V to 14V input voltage range and up to 12-A switch current. The switch current limit can be adjustable with an external resistor.

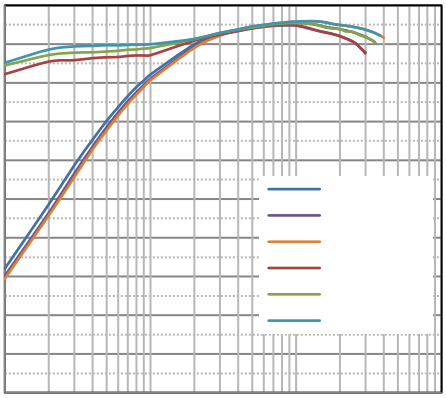
The SCT12A0 adapts constant off-time peak current control to provide fast transient. An external compensation network allows flexibility setting loop dynamics to achieve optimal transient performance at different load conditions. Using MODE pin selects either Pulse Frequency Modulation (PFM) operation or forced Pulse Width Modulation (PWM) operation. The switching frequency in PWM mode is adjustable from 200KHz to 2.2MHz by an external resistor. The device also features programmable soft-start time with an external capacitor.

The SCT12A0 monitors both output voltage and feedback voltage to protect overvoltage condition. It features cycle-by-cycle peak current limit and thermal shutdown protection when the device over loads.

The device is available in a low-profile package DFN-20L 3.5mmx4.5mmx0.75mm with enhanced thermal power pad.



Efficiency, Vout=9V



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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 2.2: Update DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT12A0DHKR	Tape & Reel	3000	12A0	20	20-Lead 3.5mm×4.5mm Plastic QFN

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
BOOT	-0.3	23.5	V
VIN, SW, VOUT, FSW	-0.3	18	V
VCC, LIM，FB， EN, SS, COMP, MODE	-0.3	5.5	V
Operating junction temperature TJ (2)	-40		

Top View: 20-Lead Plastic DFN 3.5mmx4.5mm

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FB	17	Feedback Input. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference value of 1.2V typical.
COMP	18	Output of the error amplifier and switching converter loop compensation point.
ILIM	19	Inductor peak current limit set point input. A resistor connecting this pin to ground sets current limit through low-side power FET.
AGND	20	Analog ground. Analog ground should be used as the common ground for all small signal analog inputs and compensation components. No electrical connection to PGND inside.
PGND	21	Power ground. Must be soldered directly to ground planes using multiple vias directly under the IC for improved thermal performance and electrical contact.

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.7	14	V
V_{OUT}	Output voltage range	4.5	14.6	V
T_J	Operating junction temperature	-40	125	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins (1)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

PARAMETER	THERMAL METRIC	DFN-20L	UNIT
R	Junction to ambient thermal resistance (1)	38	°C/W
R	Junction to case thermal resistance (1)	39	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT12A0 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT12A0. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

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V_{IN}=3.6V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		14	V
V_{OUT}	Output voltage range		4.5V		14.6	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising		2.6	2.7	V
	Hysteresis			200		mV
I_{SD}	Shutdown current	EN=0, No load. Measured on VIN pin		1	3	uA
I_Q	Quiescent current from VIN	EN=2V, No load, No switching. Measured on VIN pin.		1		uA
	Quiescent current from VOUT			120	200	uA
V_{CC}	Internal linear regulator	I_{VCC}=5mA, V_{IN}=6V		4.8		V
Reference and Control Loop						
V_{REF}	Reference voltage of FB	FPWM mode	1.170	1.202	1.220	V
		PSM mode	1.192	1.210	1.228	V
I_{FB}	FB pin leakage current	V_{FB}=1.2V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V		190		uS
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V		20		uA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V		20		uA
V_{COMP_H}	COMP high clamp	V_{FB}=1V， R_{ILIM}		1.5		V
V_{COMP_L}	COMP low clamp	V_{FB}=1.5V, R_{ILIM} M		0.6		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			13		
R_{DSON_L}	Low side FET on-resistance			11		
Current Limit						
I_{LIM}	Peak current limit	R_{ILIM}	10.5	12	13	A
Enable and Mode						
V_{EN}	Enable high threshold	V_{CC}=5V			1.2	V
	Enable low threshold		0.4			V
R_{EN}	Enable pull down resistance			800		
V_{MODE}	MODE high threshold	V_{CC}=5V			4	V
	MODE low threshold		1.5			V
R_{MODE}	MODE pull-up resistance			270		
I_{SS}	Soft-start charging current			5		uA
Switching Frequency						
F_{SW}	Switching frequency	R_{FSW}=301k, V_{OUT}=12V		500		kHz
t_{ON_MIN}	Minimum on-time	R_{FSW}=301k, V_{OUT}=12V		150	200	ns
T_{OFF_MIN}	Minimum off-time	R_{FSW}=301k, V_{FB}=0V		100	150	ns
Protection						
V_{OVP_VOUT}	Output overvoltage threshold	V_{OUT} rising		15.4		V
	Hysteresis			250		mV
V_{OVP_VFB}	Feedback overvoltage with respect to reference voltage	V_{FB} rising		110		%
		V_{FB} falling		105		%

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
T_{SD}	Thermal shutdown threshold	T_J rising		150		°C
	Hysteresis			20		°C

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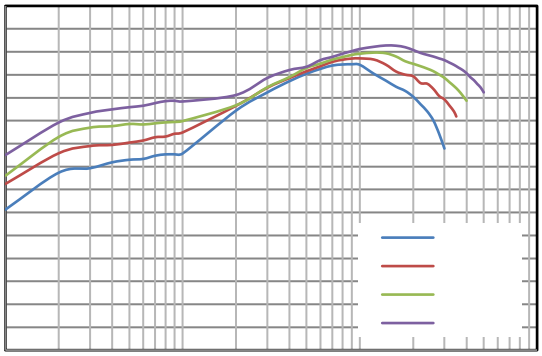

Figure 1. Efficiency, Vout=9V, fsw=560KHz, PFM

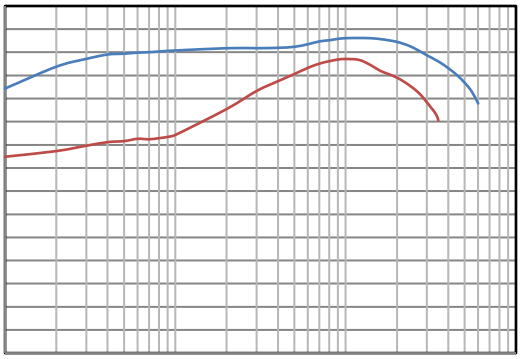

Figure 2. Efficiency, Vin=3.6V, fsw=560KHz, PFM

Figure 3. Efficiency, Vout=9V, fsw=560KHz, PWM

Figure 4. Efficiency, Vin=3.6V, fsw=560KHz, PWM

Figure 5. Switching Frequency vs FSW Resistance

Figure 6. Inductor Peak Current Limit vs RLIM Resistance

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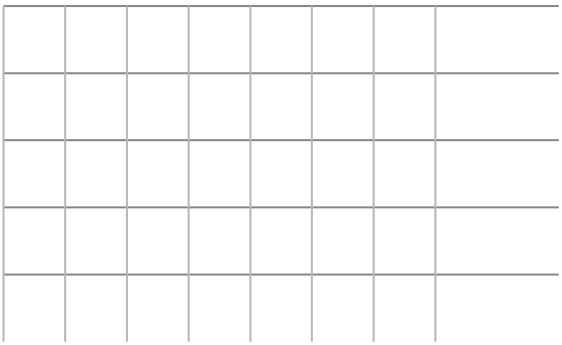

Figure 7. Frequency vs Temperature

Figure 8. Quiescent Current vs Temperature

Figure 9. Shutdown Current vs Temperature

Figure 10. Feedback Reference Voltage vs Temperature

Figure 11. Load Regulation (Vin=3.6V, Vout=9V)

Figure 12. Line Regulation

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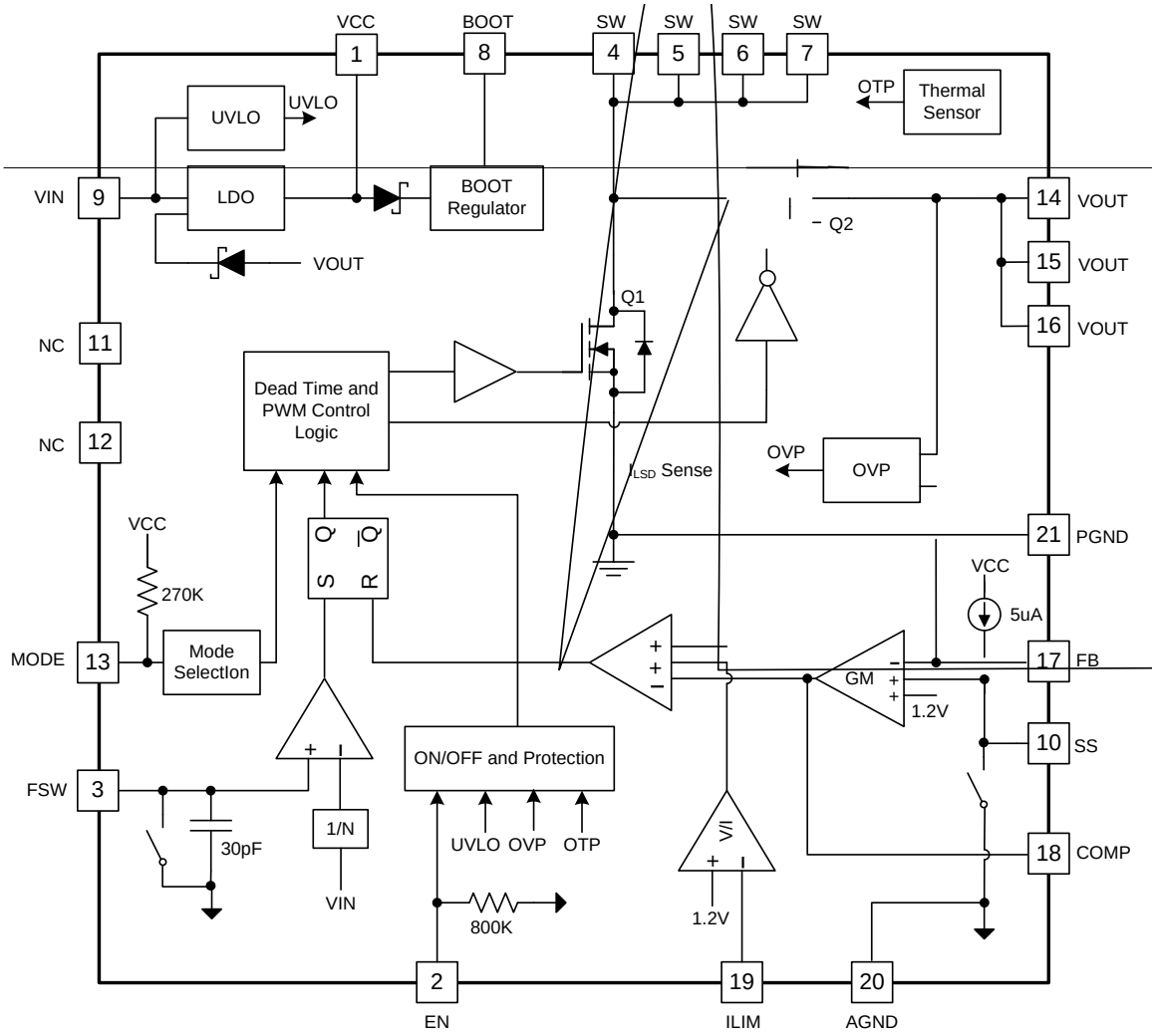

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Overview

The SCT12A0 device is a fully integrated synchronous boost converter, which regulates output voltage higher than input voltage. The constant off-time peak current mode control provides fast transient with pseudo fixed switching frequency. When low-side MOSFET Q1 turns on, input voltage forces the inductor current rise. When sensed voltage on low-side MOSFET peak current rises above the voltage of COMP, the device turns off low-side MOSFET and inductor current goes through body diode of high-side MOSFET Q2 during dead time. After dead time duration, the device turns on high-side MOSFET Q2 and the inductor current decreases. Based on Vin and Vout voltage, the device predicts required off-time and turns off high-side MOSFET Q2. This repeats on cycle-by-cycle based.

The negative voltage feedback loop regulates the FB voltage to a 1.2V reference with an internal trans-conductance error amplifier. The feedback loop stability and transient response are optimized through an external loop compensation network connected to the COMP pin.

The mode selection offers flexibility of design between forced Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM) operations. When MODE pin is connected to VCC or floats, the SCT12A0 works at PFM mode to further increase the efficiency in light load condition. If MODE pin is connected to ground, the device works in forced PWM mode with low output voltage ripple.

The quiescent current of SCT12A0 is 110uA typical under no-load condition and not switching. Disabling the device, the typical supply shutdown current is 1

A resistor connected between SW pin and the FSW pin sets the switching frequency. The wide switching frequency range of 200 kHz to 2.2 MHz offers optimization on efficiency or size of filter components.

The SCT12A0 device features adjustable soft-start time, cycle-by-cycle low-side FET current limit, over-voltage protection, and over-temperature protection.

The SCT12A0 uses two separate ground pins to avoid ground bouncing due to the high switching current through the N-channel power MOSFET. AGND pin sets the reference for all control functions. The source of the power MOSFET connects to PGND pin. Both grounds must be connected to the thermal pad on the PCB at the closest point.

VIN Power

The SCT12A0 is designed to operate from an input voltage supply range between 2.7 V to 14V. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

VCC Power

The internal VCC LDO provides the bias power supply for internal circuitries. A ceramic capacitor of no less than 1uF is required to bypass from VCC pin to ground. During starting up, input of VCC LDO is from VIN pin. Once the output voltage at VOUT pin exceeds VIN voltage, VCC LDO switches its input to VOUT pin. This allows higher voltage headroom of VCC at lower input voltage. The maximum current capability of VCC LDO is 130mA typical. No additional components or loading are recommended on this pin.

Under Voltage Lockout UVLO

The SCT12A0 features UVLO protection for voltage rails of VIN, VCC and BOOT-SW from the converter malfunction and the battery over discharging. The default VIN rising threshold is 2.6V typical at startup and falling threshold is 2.4V typical at shutdown. The internal VCC LDO dropout voltage is about 100mV and the device is disabled when VCC falling trips 2.1V typical threshold. The internal charge pump from BOOT to SW powers the gate driver to high-side MOSFET Q2. The BOOT UVLO circuit monitors the capacitor voltage between BOOT pin and SW pin. When the voltage of BOOT-SW falls below a preset threshold 3V typical, high-side MOSFET Q2 turns off. As a result, the device works as a non-synchronous boost converter.

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Enable and Start-up

When applying a voltage higher than the EN high threshold (maximum 1.2V), the SCT12A0 enables all functions and starts converter operation. To disable converter operation, EN voltage needs fall below its lower threshold (minimum 0.4V). the ground. Floating EN pin automatically disables the device.

The SCT12A0 features programmable soft start to prevent inrush current during power-up. SS pin sources an internal 5 current charging an external soft-start capacitor C_{SS} when EN pin exceeds turn-on threshold. The device uses the lower voltage between the internal voltage reference 1.2V and the SS pin voltage as the reference input voltage of error amplifier and regulates the output. The soft-start completes when SS pin voltage exceeds the internal 1.2V reference. Use equation 1 to calculate the soft-start time (10% to 90%). When EN pin is pulled low to disable the device, the SS pin will be discharged to ground.

(1)

where

-

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This current limit function is realized by detecting the current flowing through the low-side MOSFET. The current limit feature loses function in the output hard short circuit conditions. At normal operation, when the output hard shorts to ground, there is a direct path to short the input voltage through high-side MOSFET Q2 or its body diode even the Q2 is turned off. This could damage the circuit components and cause catastrophic failure at load circuit.

Once VIN is present, VOUT is moved to VIN level due to the direct path from input to output even when the device is shut down or the load is not ready. The presence of unwanted output voltage before system start up sequence could cause system latch off or malfunction.

To address the above issue, users need design external circuits for protection or choose SCT12A1 from Silicon Content Technology, which provides an option to insert an external P-channel MOSFET to disconnect output from input in application. Refer SCT12A1 data sheet for details of load disconnection feature.

Over Voltage Protection and Minimum On-time

The SCT12A0 features both VOUT pin over voltage protection and the FB pin over voltage protection. If the VOUT pin is above 15.4V typical or FB pin voltage exceeds 1.32V typical, the device stops switching immediately until the VOUT pin drops below 15.2 V or FB pin voltage drops below 1.26V. The OVP function prevents the connected output circuitry from un-predictive overvoltage. Featured feedback overvoltage protection prevents dynamic voltage spike to damage the circuitry at load during fast loading transient.

The low-side MOSFET has minimum on-time 150ns typical limitation. While the device is operating at minimum on time and further increasing Vin pushed output voltage beyond regulation point. With output and feedback over voltage protection, the converter skips pulse with turning off high-side MOSFET and prevents output running higher to damage the load.

Forced PWM and PFM Modes

Connecting MODE pin to ground, the SCT12A0 forces the device operating at forced Pulse Width Modulation (PWM) mode with pseudo-fixed switching frequency regardless loading current. Operating in PWM mode can avoid the possible audible noise caused by lower frequency in PFM mode at light load. When the load current approaches zero, the high-side MOSFET current crosses zero and sinks current from output to maintain the constant output. Hence power efficiency in light load is much lower than heavy load.

Floating MODE pin or connecting MODE pin to VCC, the SCT12A0 works at Pulse Frequency Modulation (PFM) mode to improve the power efficiency in light load. As the load current decreasing, the COMP pin voltage decreases as resulting the inductor current down. With the load current further decreasing, the COMP pin voltage decreases and be clamped to a voltage corresponding to the ILIM/12. The converter extends the off time of high-side MOSFET Q2 to reduce the average delivered current to output. The switching frequency is lower and varied depending on loading condition. In PFM mode, the peak inductor current is fixed at around 1A and the output voltage is regulated 0.7% higher than the setting output voltage. When the inductor current decreased to zero, zero-cross detection circuitry on high-side MOSFET Q2 forces the Q2 off until the beginning of the next switching cycle. The boost converter does not sink current from the load at light load.

Thermal Shutdown

Once the junction temperature in the SCT12A0 exceeds 150^{O}C, the thermal sensing circuit stops switching until the junction temperature falling below 130C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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Typical Application

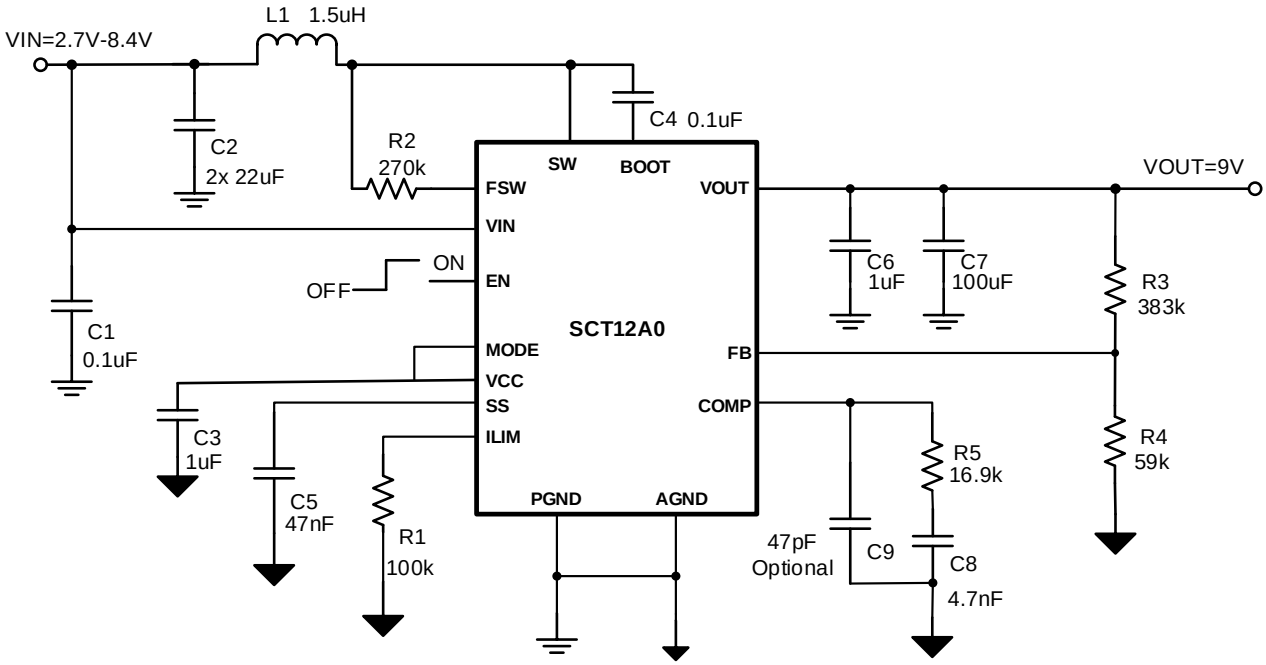

Figure 13. One Cell Battery Input, 9V/3A (30W) Output

Design Parameters

Design Parameters	Example Value
Input Voltage	3.0V to 4.2V
Output Voltage	9V
Output Current	3A
Output voltage ripple (peak to peak)	100mV
Switching Frequency	560 kHz
Operation Mode	PFM

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Switching Frequency

The resistor connected from FSW to SW sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation 2. High frequency can reduce the inductor and output capacitor size with the tradeoff of more thermal dissipation and lower efficiency.

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 90 ns
- C_{FREQ} = 34 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Table 1. R_{FSW} Value for Common Switching Frequencies (Vin=3.6V, Vout=9V, Room Temperature)

Fsw	R_{FSW}
200 KHz	750
350 KHz	
520 KHz	270
730 KHz	
1000 KHz	127
2000 KHz	

Peak Current Limit

Using the correct external resistor at ILIM pin sets the peak input current. Table 2 shows the resistor value for inductor peak current limit. For a typical current limit of 12A, the resistor value is 100 . The minimum current limit must be higher than the required peak switch current at lowest input voltage and the highest output power not to hit the current limit and still regulate the output voltage.

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance of ILIM pin to ground

Table 2. R_{LIM} Value for Inductor Peak Current (Vin=3.6V, Vout=9V, L=1.5uH, Room Temperature)

I_{LIM}	R_{LIM}
12 A	100
8 A	154
6.3A	200
4.4A	301

Output Voltage

The output voltage is set by an external resistor divider R3 and R4 in typical application schematic. A minimum current of typical 20uA flowing through feedback resistor divider gives good accuracy and noise covering. The value of R3 can be calculated by equation 4.

(4)

where:

- V_{REF} is the feedback reference voltage, typical 1.2V

Table 3. Feedback Resistor R_3 R_4Value for Output Voltage (Room Temperature)

V_{OUT}	R_3	R_4
5 V	187	59
9 V	383	59
12 V	536	59

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Inductor Selection

The performance of
and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a boot converter, calculate the inductor DC current as in equation 5

(5)

Where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
-

Calculate the inductor current peak-to-peak ripple, I_{LPP}, as in equation 6.

(6)

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore the peak switching current of inductor, I_{LPEAK}, is calculated as in equation 7.

(7)

Set the current limit of the SCT12A0 higher than the peak current I^{LPEAK} and select the inductor with the saturation current higher than the current limit.

The the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. T inductance, DCR and ESR resistance, and its footprint. Shielded inductors typically have higher DCR than unshielded inductors. Table 4 lists recommended inductors for the SCT12A0. Verify whether the recommended inductor Veri

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calculations and bench evaluation. In this application, the WB's inductor CDMC8D28NP-1R2MC is used on SCT12A0 evaluation board.

Table 4. Recommended Inductors

Part Number	L (uH)	DCR Max d	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
WE-HCI SMD 7443552150	1.5	5.3	17 / 14	10.5 x 10.2 x 4.0	WurthElektronix
CDMC8D28NP-1R2MC	1.2	7.0	12.2 / 12.	9.5 x 8.7 x 3.0	Sumida

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A 0.1 recommended to be placed as close as possible to the VIN pin of the SCT12A0. A ceramic capacitor of more than 1.0 internal LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasite inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, 2x 22 recommended for most applications. Choose the right capacitor value carefully

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Layout Guideline

The regulator could suffer from instability and noise problems without careful layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be close to the VIN pin and GND pin to reduce the input supply ripple. The placement and ground trace for C6 are critical for the performance of SW ringing voltage. Place capacitor C6 as close to VOUT pin and power ground pad as possible to reduce high frequency ringing voltage on SW pin. Short NC pins to power ground pad directly to reduce the ground trace impedance of C6.

The layout should also be done with well consideration of the thermal. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias under the thermal pad. The bottom layer is a large ground plane connected to the PGND plane and AGND plane on top layer by vias. Since thermal pad is electrical power ground of the device, improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. It is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss through the vias is of concern, plugging or tenting can be used to achieve a repeatable process.

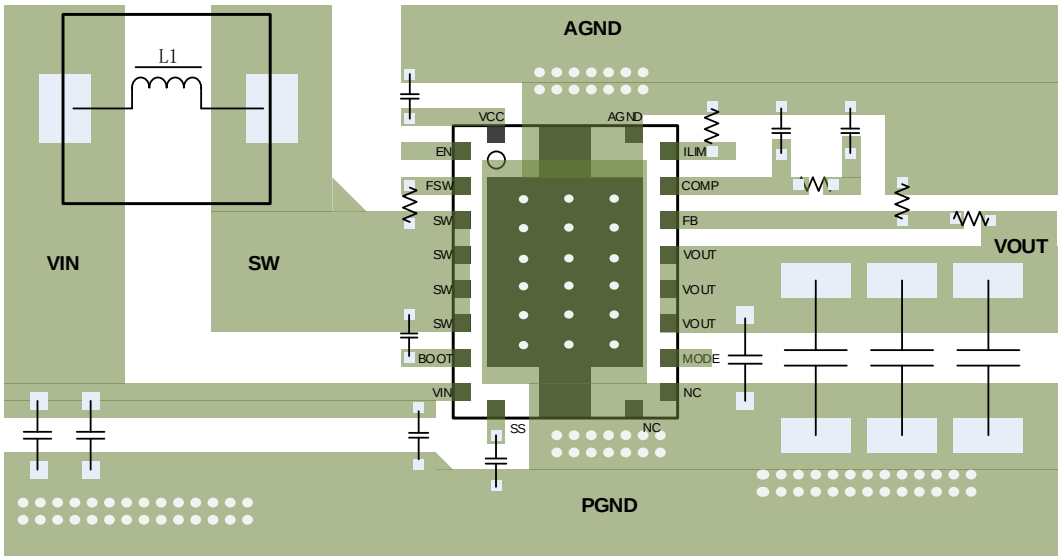

Figure 20. PCB Layout Example Bottom Layer

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 18.

(18)

where

- T_A is the maximum ambient temperature for the application.
- R is the junction-to-ambient thermal resistance given in the Thermal Information table.

SCT12A0 DFN package includes a thermal pad that improves the thermal capabilities of the package. The real junction-to-ambient thermal resistance R of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

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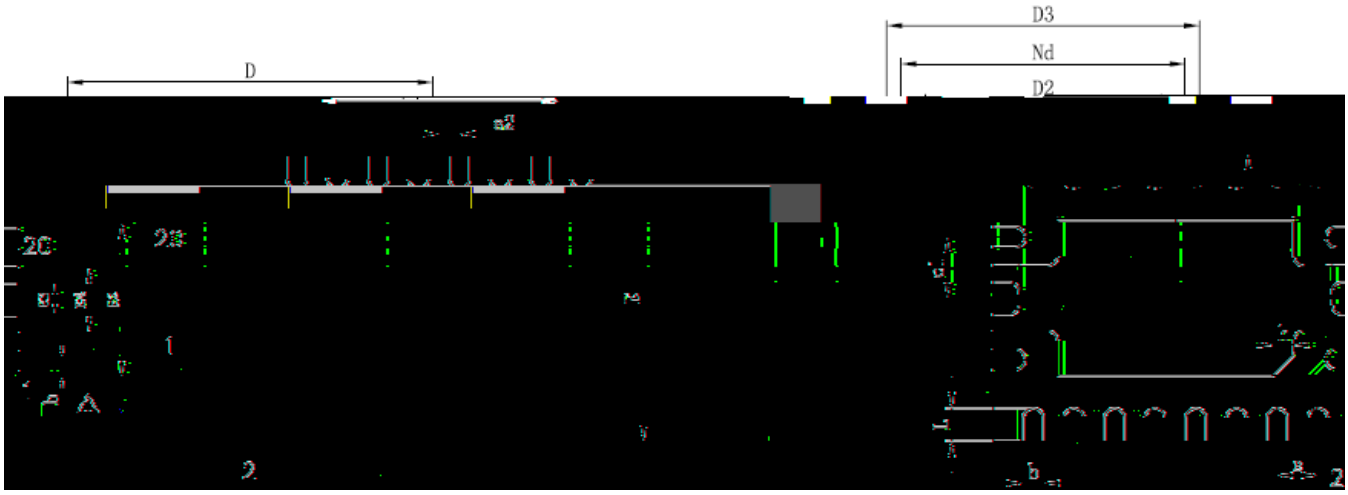
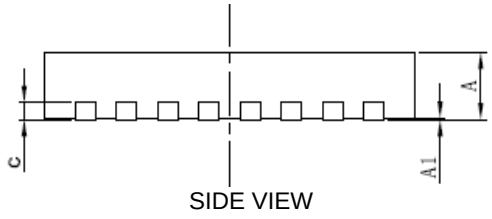


TOP VIEW

BOTTOM VIEW



SIDE VIEW

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.40	4.50	4.60
D2	3.10	3.20	3.30
D3	3.85REF		
e	0.50BSC		
e1	0.75BSC		
e2	0.25BSC		
Nd	3.50BSC		
E	3.40	3.50	3.60
E2	2.10	2.20	2.30
E3	0.35REF		
E4	0.75REF		
L	0.35	0.40	0.45
h	0.20	0.25	0.30

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REEL DIMENSIONS

Reel Width	A	B	C	D	t
12	Ø329±1	12.8±1	Ø100±1	Ø13.3±0.3	2.0±0.3

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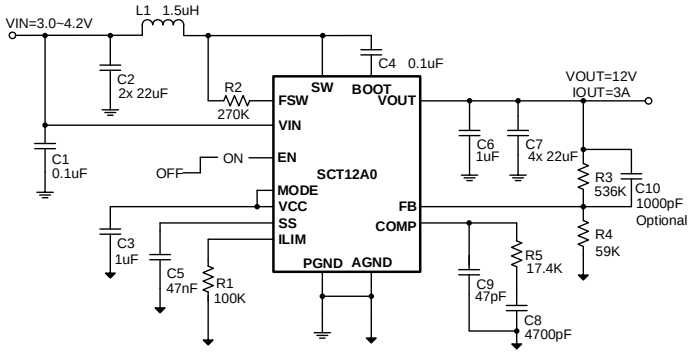
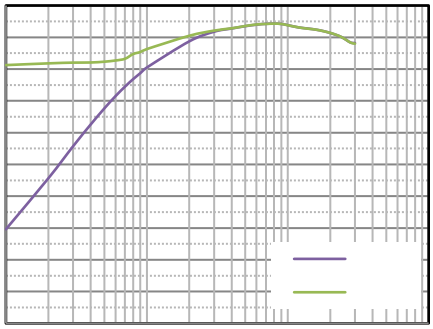
12V Output, Synchronous Boost Converter



Efficiency, Vin=3.6V



PART NUMBERS	DESCRIPTION	COMMENTS
SCT12A1	30W Fully-integrated Synchronous Boost Converter with Load Disconnection	Vin=2.7V-14V, 12A switch current Load disconnection control to an external PMOS with high-side current sensing to protect • Damage of circuit components and cause catastrophic failure at load during hard short. • Presence of unwanted output voltage before start up sequence causing system to latch off or malfunction.

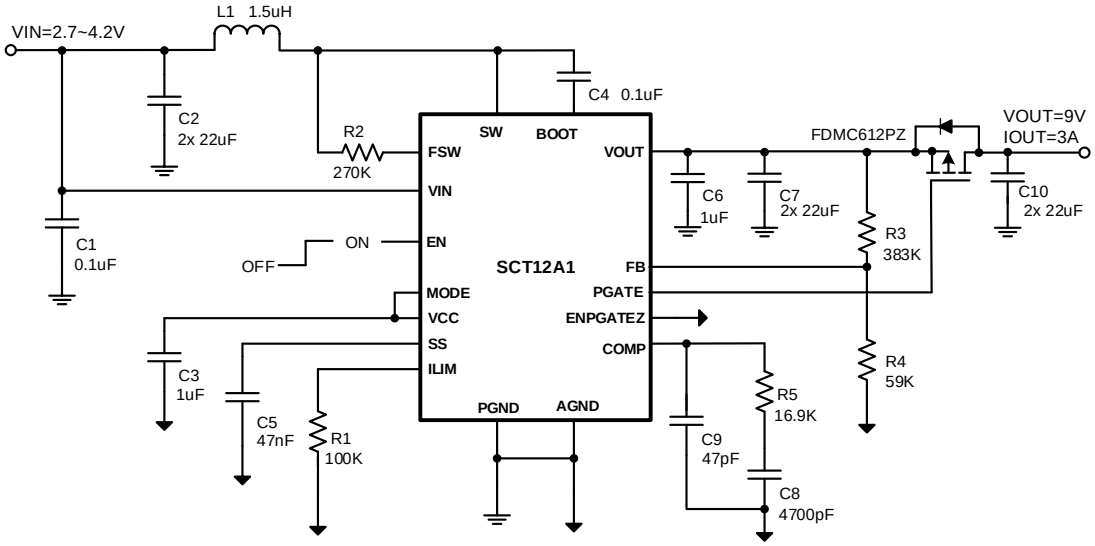


Figure 20. SCT12A1 Typical Application

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